

METHOD OF DETERMINING DATA TRANSFER SPEED
IN DATA TRANSFER APPARATUS

BACKGROUND OF THE INVENTION

5 The present invention relates to a method of determining a data transfer speed, and more particularly, to a method of determining a data transfer speed in an interface apparatus in conformity to IEEE1394.

10 The IEEE1394 protocol is known as a standard for an interface for transferring data such as audio data, image data and so on at a high speed between a personal computer and a peripheral device. The IEEE1394 protocol is advantageous in its high degree of freedom in bus topology which permits a daisy chain topology, a star topology, and so
15 on.

A Data-Strobe Link (DS-LINK) coding scheme is employed for a transfer format of the IEEE1394 protocol. The DS-LINK coding scheme encodes a clock signal and a data signal to generate an encoded data signal and a strobe signal. When
20 data having the same value are continuously output, the continuity of the data is represented by changing the value of the strobe signal. A clock signal is generated by performing an exclusive OR operation of the encoded data and the strobe signal.

25 The IEEE1394 protocol standardizes three data transfer speeds: 100 Mbps, 200 Mbps and 400 Mbps. Therefore, for transferring data between devices, a data transfer speed must be notified to the destination device by speed signaling each time data packets are transmitted. The device, that is
30 notified of the data transfer speed, repeatedly transfers the received data packets to the next device at the notified data transfer speed.

The speed signaling is performed by supplying a bias

signal to a signal line for the strobe signal of a 1394 cable. The bias signal is supplied for a fixed period (data prefix period) before the transmission of data packets. One of the data transfer speeds 100 Mbps, 200 Mbps, and 400 Mbps is 5 specified depending on the analog level of the bias signal. A receiver recognizes a data transfer speed by detecting the analog level of the bias signal.

The recognition of the data transfer speed requires a strict detection of the analog level of the bias signal. 10 Therefore, in a poor use environment which may involve an unstable power supply, and so on, an error is likely to occur in the detection of the analog level of the bias signal.

Also, the detection of the analog level of the bias signal requires an analog-to-digital converter circuit which 15 has a relatively large circuit area. Therefore, a larger semiconductor integrated circuit device must be built in an interface controller.

Further, negotiations for a data transfer speed performed in IEEE1394 impede an improvement in transfer 20 efficiency.

SUMMARY OF THE INVENTION

It is a first object of the present invention to provide a method of determining a data transfer speed that reliably 25 determines a data transfer speed.

It is a second object of the present invention to provide a method of determining a data transfer speed that has an improved data transfer efficiency.

In a first aspect of the invention, a method of 30 determining a transfer speed of an encoded data signal including a clock signal and a data signal is provided. First, the encoded data signal is decoded to generate a decoded clock signal. Then, a data transfer speed is

determined using the decoded clock signal.

In a second aspect of the present invention, a method of transferring an encoded data signal including a clock signal and a data signal is provided. First, the encoded data signal is decoded to generate a decoded data signal and write clock signal. The decoded data signal is stored in a memory in accordance with the write clock signal. A transfer speed of the encoded data signal is determined using the write clock signal. A read clock signal, which has a frequency corresponding to the determined data transfer speed, is generated. Then, the decoded data signal stored in the memory is read in accordance with the read clock signal. The read decoded data signal and the read clock signal are encoded to generate an encoded data signal.

In a third aspect of the present invention, an apparatus for transferring an encoded data signal including a clock signal and a data signal is provided. The apparatus includes an decoder circuit for decoding the encoded data signal to generate a decoded data signal and write clock signal. A memory is connected to the decoder circuit to store the decoded data signal in accordance with the write clock signal. A transfer speed determining circuit determines a transfer speed of the encoded data signal in accordance with the write clock signal. The transfer speed determining circuit generates a read clock signal having a frequency corresponding to the determined transfer speed. The decoded data signal is read from the memory in accordance with the read clock signal. An encoder circuit is connected to the memory and the transfer speed determining circuit to encode the decoded data signal and the read clock signal to generate the encoded data signal.

Other aspects and advantages of the invention will become apparent from the following description, taken in

conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

5 The invention, together with objects and advantages thereof, may best be understood by reference to the following description of the presently preferred embodiments together with the accompanying drawings in which:

10 Fig. 1 is a schematic block diagram illustrating a data transfer system of one embodiment of the present invention;

Fig. 2 is a schematic block circuit diagram illustrating an interface device for a personal computer of the system of Fig. 1;

15 Fig. 3 is a schematic block diagram illustrating a data transfer speed control circuit of the interface device of Fig. 2;

Fig. 4 is a schematic block diagram illustrating a FIFO circuit of the data transfer speed control circuit of Fig. 3;

20 Fig. 5 is a schematic block diagram illustrating a clock signal generating circuit of the data transfer speed control circuit of Fig. 3;

Fig. 6 is a timing chart for explaining the operation of the FIFO circuit of Fig. 4;

25 Fig. 7 is a schematic block diagram illustrating a determining circuit of the data transfer speed control circuit of Fig. 3; and

Fig. 8 is a flow chart showing the operation of the data transfer speed control circuit of Fig. 3.

30 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A data transfer apparatus in one embodiment of the present invention will hereinafter be described with reference to the drawings.

As illustrated in Fig. 1, a data transfer system 100 in conformity to the IEEE 1394 protocol includes a personal computer 1, a digital video camera 2, and a printer 3. Each of the personal computer 1, digital video camera 2 and printer 3 includes an interface device for performing a data transfer in conformity to the IEEE1394 protocol, and is interconnected via IEEE1394 bus cables 4, 5 to constitute a daisy chain type bus topology. More specifically, a first input/output port 1a of the personal computer 1 is connected to an input/output port 2a of the digital video camera 2 via the bus cable 4, while a second input/output port 1b of the personal computer 1 is connected to an input/output port 3a of the printer 3 via the bus cable 5.

The interface device 10 of the personal computer 1 is described in Fig. 2. Since the interface devices of the digital video camera 2 and the printer 3 are identical in configuration to the interface device of the personal computer 1, description thereon is omitted.

As illustrated in Fig. 2, the interface device 10 includes a physical layer processing circuit 11, which has a first DS decoder/encoder 12 and a second DS decoder/encoder 13, and a data transfer speed control circuit 14.

The first DS decoder/encoder 12 is connected to the bus cable 4 via the first input/output port 1a to communicate data with the digital video camera 2. The first DS decoder/encoder 12 decodes DS-LINK encoded data (a data signal and a strobe signal) supplied from the digital video camera 2 to generate a data signal D1 and a DS clock signal CL1 as a write clock signal.

The first DS decoder/encoder 12 receives a read data signal D2 and a read clock signal CL2 supplied from the data transfer speed control circuit 14, each of which is generated by an internal logic circuit (not shown). The first DS

decoder/encoder 12 encodes the read data signal D2 and the read clock signal CL2 in accordance with the DS-LINK coding scheme to generate a data signal and a strobe signal. The data signal and the strobe signal are supplied to the digital 5 video camera 2 via the bus cable 4.

The second DS decoder/encoder 13 is connected to the bus cable 5 via the second input/output port 1b to communicate data with the printer 3. The second DS decoder/encoder 13 decodes DS-LINK encoded data (a data signal and a strobe 10 signal) supplied from the printer 3 to generate the DS clock signal CL1 and the DS data signal D1.

The second DS decoder/encoder 13 receives the read data signal D2 and the read clock signal CL2, which are supplied from the data transfer speed control circuit 14 and are 15 generated by the internal logic circuit (not shown). The second DS decoder/encoder 13 encodes the read data signal D2 and the read clock signal CL2 in accordance with the DS-LINK coding scheme to generate a data signal and a strobe signal. The data signal and the strobe signal are supplied to the 20 printer 3 via the bus cable 5.

The data signal and the strobe signal, which are supplied from the digital video camera 2, are transferred to the printer 3 via the first DS decoder/encoder 12, data transfer speed control circuit 14 and second DS 25 decoder/encoder 13, which is refereed as a repeat transfer.

The data signal and the strobe signal, which are supplied from the printer 3, are transferred to the digital video camera 2 via the second DS decoder/encoder 13, data transfer speed control circuit 14 and first DS 30 decoder/encoder 12, which is refereed as the repeat transfer.

The data signal and the strobe signal, which are supplied from the digital video camera 2, are transferred to an internal logic circuit of the personal computer 1 as the

read data signal D2 and the read clock signal CL2 via the first DS decoder/encoder 12 and the data transfer speed control circuit 14.

The read data signal D2 and the read clock signal CL2, 5 which are generated by the personal computer 1, are transferred to the digital video camera 2 as a data signal and a strobe signal via the first DS decoder/encoder 12.

The data signal and the strobe signal, which are supplied from the printer 3, are supplied to the internal 10 logic circuit of the personal computer 1 as the read data signal D2 and the read clock signal CL2 via the second DS decoder/encoder 13 and the data transfer speed control circuit 14.

The read data signal D2 and the read clock signal CL2, 15 which are generated by the personal computer 1, are transferred to the printer 3 as a data signal and a strobe signal via the second DS decoder/encoder 13.

As illustrated in Fig. 3, the data transfer speed control circuit 14 includes an oscillator circuit 21, a FIFO (First In First Out) circuit 22, a timer 23, a determining circuit 24, and a clock signal generator circuit 25. The timer 23, the determining circuit 24 and the clock signal generator circuit 25 form a transfer speed determining circuit.

The oscillating circuit 21 generates a reference clock signal CLX at 400 MHz which is supplied to the timer 23 and the clock signal generator circuit 25.

The FIFO circuit 22 sequentially stores the DS data signal D1 bit by bit in accordance with the DC clock signals CL1 from the first and second DS decoder/encoders 12, 13. 30 Specifically, as illustrated in Fig. 8, the FIFO circuit 22 stores the DS data signal D1 in accordance with the DS clock signal CL1 while the DS clock signal CL1 and the DS data

signal D1 are being supplied, in accordance with steps S101, S102.

The FIFO circuit 22 sequentially reads the stored DS data signal D1 in accordance with the read clock signal CL2, 5 bit by bit, to output a read data signal D2.

As illustrated in Fig. 4, the FIFO circuit 22 includes a memory cell circuit 31, a write pointer 32, a read pointer 33, and a pointer comparator 34. The write pointer 32 shifts a write address in the memory cell circuit 31 in accordance 10 with the DS clock signal CL1. The memory cell circuit 31 stores one bit of the DS data signal D1 in accordance with the write address from the write pointer 32, each time the write address is shifted.

The read pointer 33 shifts a read address of the memory 15 cell circuit 31 in accordance with the read clock signal CL2. The memory cell circuit 31 outputs one bit of the DS data signal D1 written therein as a read data signal D2 in accordance with the read address from the read pointer 33, each time the read address is shifted.

20 The pointer comparator 34 receives a write address pointed by the write pointer 32 and a read address pointed by the read pointer 33 to recognize a write situation and a read situation of the DS data signal D1 in the memory cell circuit 31 based on the write and read addresses.

25 The pointer comparator 34 counts the number of bits of the DS data signal D1 transmitted from the digital video camera 2 (or from the printer 3) and outputs a timer control signal TE, which has a low potential (L level), as illustrated in Fig. 6, while eight bits of the DS data signal 30 D1 are written. More specifically, the pointer comparator 34 outputs the timer control signal TE having the L level when the DS data signal D1 and the DS clock signal CL1 of the digital video camera 2 (or the printer 3) are supplied from

the first DS decoder/encoder 12 (or from the second DS decoder/encoder 13) in a state where no DS data signal D1 has been written into the memory cell circuit 31 and the write address is coincident with the read address. Thus, the DS 5 data signal D1 is sequentially written into the memory cell circuit 31 in accordance with the DS clock signal CL1. At this time, since the read clock signal CL2 is not output, the read pointer 33 is inoperative.

When eight bits of the DS data signal D1 have been 10 written (when a difference between the write address and the read address reaches "8"), the pointer comparator 34 raises the timer control signal TE from the L level to a high potential (H level).

The timer 23 counts a time (count value X) required to 15 write eight bits of the DS data signal D1 into the memory cell circuit 31 in response to the timer control signal TE. More specifically, the timer 23 is reset at the time the timer control signal TE falls to the L level and starts counting the reference clock signal CLX of 400 MHz. As shown 20 in steps S103, S104 in Fig. 8, the timer 23 stops the counting operation when the timer control signal TE rises to the H level and outputs the count value X.

The determining circuit 24 receives the count value X from the timer 23 and determines a transfer speed of data 25 transferred to the digital video camera 2 (or the printer 3) based on the count value X. Specifically, the determining circuit 24 determines that the data transfer speed is 400 MHz when the count value is less than "10". The determining circuit 24 determines that the data transfer speed is 200 MHz 30 when the count value X is equal to or more than "10" and less than "18". Further, the determining circuit 24 determines that the data transfer speed is 100 MHz when the count value X is equal to or more than "18". A determination value used

by the determining circuit 24 has been stored in the predetermined determination table (not shown), and the determination is made based on the determination value.

The determining circuit 24 determines that the data transfer speed is 400 MHz even when the count value X is "9", "8" or "7". In other words, the count value X within the predetermined range corresponds to one data transfer speed. More exactly, when the transfer speed of the DS data signal D1 is 400 MHz, the count value X is "8". When the transfer speed of the DS data signal D1 is 200 MHz, the count value X is "16". When the transfer speed of the DS data signal D1 is 100 MHz, the count value X is "32". However, the transfer speed of the digital video camera 2 (or the printer 3) may become slightly higher or lower, for example, than 400 MHz for some reason. To compensate for an error in the transfer speed, the embodiment provides a certain margin to the count value. With this expedient, the data transfer speed can be correctly determined even if the count value X is not "8".

As illustrated in Fig. 7, the determining circuit 24 includes a comparison value setting circuit 40, a first and a second comparator circuit 41, 42, and an encoder 43. The comparison value setting circuit 40 supplies a first comparison value Z1 and a second comparison value Z2 to the first comparator circuit 41 and the second comparator circuit 42, respectively. In this embodiment, the first comparison value Z1 is set to "10", while the second comparison value Z2 is set to "18".

The first comparator circuit 41 compares the count value X of the timer 23 with the first comparison value Z1 to generate a first comparison result signal having the L level when the count value X is less than the first comparison value Z1 ($X < Z1$). The first comparison circuit 41 generates the first comparison result signal having the H level when

the count value X is equal to or more than the first comparison value Z1 ($X \geq Z1$).

The second comparator circuit 42 compares the count value X of the timer 23 with the second comparison value Z2 to generate a second comparison result signal having the L level when the count value X is less than the second comparison value Z2 ($X < Z2$). The second comparator circuit 42 generates the second comparison result signal having the H level when the count value X is equal to or more than the second comparison value Z2 ($X \geq Z2$).

The encoder 43 receives the first and second comparison result signals from the first and second comparator circuits 41, 42 and determines a data transfer speed based on the first and second comparison result signals Z1, Z2 to generate a determination result Y. More specifically, the encoder 43 generates the determination result Y indicating that the data transfer speed is 400 MHz when the first and second comparison result signals have the H level. The encoder 43 generates the determination result Y indicating that the data transfer speed is 200 MHz when the first comparison result signal has the H level and the second comparison result signal has the L level. Further, the encoder 43 generates the determination result Y indicating that the data transfer speed is 100 MHz when the first and second comparison result signals have the L level.

The clock signal generator circuit 25 divides the reference clock signal CLX of 400 MHz in accordance with the determination result Y from the determining circuit 24 to generate the read clock signal CL2. Specifically, when the determination result Y indicates 100 MHz, the clock signal generator circuit 25 divides the reference clock signal CLX by four to generate the read clock signal CL2 of 100 MHz. When the determination result Y indicates 200 MHz, the clock

signal generator circuit 25 divides the reference clock signal CLX by two to generate the read clock signal CL2 of 200 MHz. Further, when the determination result Y indicates 400 MHz, the clock signal generator circuit 25 outputs the 5 read clock signal CL2 of 400 MHz without dividing the reference clock signal CLX. Thus, the clock signal generator circuit 25 generates the read clock signal CL2 which has a frequency corresponding to the data transfer speed determined by the destined digital video camera 2 (or printer 3).

10 As illustrated in Fig. 5, the clock generator circuit 25 includes a 1/4 divider 35, a 1/2 divider 36, and a selector circuit 37. The 1/4 divider 35 divides the reference clock signal CLX of 400 MHz by four to supply the selector circuit 37 with a 1/4 divided signal. The 1/2 divider 36 divides the 15 reference clock signal CLK of 400 MHz by two to supply the selector 37 with a 1/2 divided signal.

20 The selector circuit 37 selects any one of the reference clock signal CLX, 1/2 divided signal and 1/4 divided signal in accordance with the determination result Y from the determining circuit 24 and outputs the selected signal as the read clock signal CL2. The selector circuit 37 does not output the read clock signal CL2 when no DS data signal D1 is written in the memory cell circuit 31 and when the write address is coincident with the read address. In other words, 25 the selector 37 waits until it is supplied with the determination result Y from the determining circuit 24.

Thus, as shown in step S105 of Fig. 8, the read clock signal CL2 is supplied to the FIFO circuit 22 after eight bits of the DS data signal D1 from the digital video camera 2 30 (or from the printer 3) have been written to the memory cell circuit 31. In other words, after eight bits of the DS data signal D1 from the digital video camera 2 (or from the printer 3) have been written, the data is read from the FIFO

circuit 22 in accordance with the data transfer speed of the transmitter side.

In the repeat transfer, the read data signal D2 read from the FIFO circuit 22 is supplied to the first DS decoder/encoder 12 (or the second DS decoder/encoder 13) together with the read clock signal CL2. In other words, when the data is destined for the digital video camera 2, the read data signal D2 and the read clock signal CL2 are supplied to the first DS decoder/encoder 12. When the data is destined for the printer 3, the read data signal D2 and the read clock signal CL2 are supplied to the second DS decoder/encoder 13.

The first and second DS decoder/encoders 12, 13 encode the read data signal D2 and the read clock signal CL2 in accordance with the DS-LINK coding scheme and transfers the encoded data signal and a strobe signal to the digital video camera 2 (or to the printer 3).

The interface device 10 of the embodiment has the following advantages:

(1) Based on a measured time (count value X) required to store eight bits of the DS data signal D1 in the FIFO circuit 22 in accordance with the DS clock signal CL1, the data transfer speed of the digital video camera 2 (or the printer 3) is determined. It is therefore possible to recognize the data transfer speed of the digital video camera 2 (or the printer 3) without detecting the analog level of the bias signal supplied for the predetermined period before transmission of the data signal for speed signalling in the IEEE1394 protocol.

Moreover, when the data transfer speed is recognized, the read clock signal CL2 corresponding to the data transfer speed is immediately generated, and the DS data signal D1 is read from the FIFO circuit 22 in accordance with the read

clock signal CL2 and transferred to a destination device via the first DS decoder/encoder 12 (or the second DS decoder/encoder 13). Thus, in the repeat transfer of the IEEE1394, the data signal is reliably transferred at the data transfer speed of the digital video camera 2 (or the printer 3) on the transmission side.

5 Since all devices on the network topology include the interface device 10, a plurality of devices can mutually perform the repeat transfer of the IEEE1394 protocol, while 10 omitting the speed signaling in IEEE1394. This results in elimination of the speed signaling phase in IEEE1394, so that 15 the data transfer efficiency is improved.

(2) Since the recognition of the data transfer speed does not involve detecting the analog level of the bias 15 signal, no analog-to-digital converter circuit is required for detecting the analog level of the digital signal. Therefore, a smaller semiconductor integrated circuit device may be built in the interface controller.

(3) An actual data transfer speed is measured based on 20 an encoded data signal and a strobe signal supplied from the digital video camera 2 (or the printer 3) on the transmission side to recognize the data transfer speed of the digital video camera 2 (or the printer 3). This ensures that the data transfer speed is correctly determined, as compared with 25 the determination of the analog level of the bias signal, without depending on a particular environment in which the data transfer apparatus is used.

(4) The FIFO circuit 22 includes the comparator 34 for 30 generating the timer control signal TE, which has the L level, indicative of a period in which eight bits of the DS data signal D1 are stored in the FIFO circuit 22 in accordance with the DS clock signal CL1. The comparator 34 occupies a circuit area smaller than a dedicated circuit which is

provided exclusively for generating the timer control signal TE.

(5) The timer 23 measures a time taken to store eight bits of the DS data signal D1 by counting the reference clock signal CLX of 400 MHz, which is output from the oscillator circuit 21, while the timer control signal TE remains at L level. Therefore, a dedicated oscillator circuit is not required for generating a clock signal, so that the circuit area is reduced.

10 (6) The clock signal generator circuit 25 generates the read clock signals CL2 of 400 MHz, 200 MHz or 100 MHz from the reference clock signal CLX of 400 MHz. Therefore, no independent oscillator circuit is required for each frequency, so that the circuit area is reduced.

15 (7) The determining circuit 24 determines that the data transfer speed is 400 MHz when the count value X is less than 10; the data transfer speed is 200 MHz when the count value X is equal to or more than 10 and less than 18; and the data transfer speed is 100 MHz when the count value X is equal to 20 or more than 18. Thus, even if the data transfer speed of a device at the transmission side fluctuates slightly for some reason, a reliable determination is provided without causing disabled determination or erroneous determination.

25 It should be apparent to those skilled in the art that the present invention may be embodied in many other specific forms without departing from the spirit or scope of the invention. Particularly, it should be understood that the invention may be embodied in the following forms.

30 (a) A time required to store less than eight bits of the DS data signal D1, such as four bits, six bits, or the like may be measured. In this case, a time required for the determination is reduced.

The foregoing embodiment is applied to the DS data

signal D1, the minimum unit (packet) of which is eight bits. When it is ensured that the data signal D1 in the form of a packet including eight bits or more is transferred at all times, a time required to store a data signal of bits larger than eight may be measured.

(b) A counter for counting the DS clock signal CL1 may be provided instead of the pointer comparator 34. In this case, the timer 23 performs a counting operation until the counter counts up to the predetermined number of clocks.

(c) The reference clock signal CLX is not limited to 400 MHz, but may employ a clock signal lower than 400 MHz such as, for example, 200 MHz, 100 MHz or the like, or a clock signal higher than 400 MHz such as 500 MHz, 600 MHz or the like.

(d) In place of the pointer comparator 34 and the determination circuit 24, the data transfer speed may be determined by software. For example, using a storage device which previously stores data on the determination results Y for the count time X, data of the determination result Y corresponding to a particular count time X of the timer 23 may be read from the storage device in accordance with a program to determine the data transfer speed.

Therefore, the present examples and embodiments are to be considered as illustrative and not restrictive and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalence of the appended claims.